## 19.5 A 4.1mW 79dB-DR 4th-order Source-Follower-Based Continuous-Time Filter for WLAN Receivers

S. D'Amico[1], M. Conta[2], A. Baschirotto[1]

[1]University of Lecce, Lecce, Italy
[2]RFDomus, Irvine, CA

The increasing demands of portable terminals for wireless communication with improved services forces the development of lower power circuits. The power consumption of each block is of fundamental importance since reducing the power would make power available for new services [1, 2, 3]. The baseband continuous-time filter in the receiver is addressed here. Active-*RC* and active-$G_m$-*RC* [2] filters guarantee high linearity, but consume more power than $G_m$-*C* [1] filters; however, $G_m$-*C* filters suffer from reduced linearity. A source-follower-based solution is presented, which allows a significant power reduction while guaranteeing the required linearity is maintained.

Three implementations of the basic fully-differential 2nd-order lowpass filter are shown in Fig. 19.5.1. Figure 19.5.1(a) presents an optimized single-branch fully-differential structure and operates as a 'composite' source-follower (ideally with unity dc-gain). A positive feedback (always stable due to the presence of the MOS output impedance) internal to the source follower ($M_4$ & $M_3$) allows the synthesis of complex-poles. If the transistors' output conductances are much larger than their transconductances, and $g_{m1} = g_{m4} = g_{m2} = g_{m3}$, the filter transfer function is:

$$H(s) = -\frac{1}{s^2 \cdot \frac{C_1 \cdot C_2}{g_{m1}^2} + s \cdot \frac{C_1}{g_{m1}} + 1}$$

The filter parameters (the pole frequency $\omega_n$, the quality factor $Q$, and the dc-gain $K$) are:

$$\omega_0 = 2 \cdot \pi \cdot f_0 = \frac{g_{m1}}{\sqrt{C_1 \cdot C_2}};\ Q = \sqrt{\frac{C_2}{C_1}};\quad |K| = 1;$$

This structure presents the key advantage of the source-follower: as with any feedback structure, its linearity improves with a larger closed-loop gain (given by $g_m \cdot R_{out}$, where $R_{out}$ is the $I_o$ current-source output impedance and $g_m$ is the input-device transconductance). Thus a larger $g_m$ value (achieved for a lower $V_{ov}$) gives a better linearity. This basic conclusion completely differs from active-*RC* and $G_m$-*C* filters, where the linearity is improved for a larger $V_{ov}$ of the input devices Breaking the dependence between $V_{ov}$ and linearity has large direct impact on the filter performance. Minimizing $V_{ov}$ corresponds to reducing the current level (and the power consumption) required to achieve a given $g_m$ value which, in turn, yields a significant power reduction for the same linearity. In addition, the $1/V_{ov}$ dependence of $g_m$ magnifies this effect. Achieving a large $g_m$ with a lower current also leads to excellent noise performance and enables the use of a larger capacitor for a given pole frequency, increasing robustness of the performance with respect to parasitic capacitance. Since the target is to achieve a high $g_m$ despite the low $V_{ov}$, the structure also features large linearity with BJT devices, as shown in Fig. 19.5.1(b). Fig. 19.5.1(c) shows the MOS folded version of the circuit. The linearity of all three circuits is set by the operation of $M_3$ and $M_4$ (which may operate in the linear region, enabling a swing of about $V_{TH} + V_{ov}$) and by the high-impedance of the current source $I_o$ (which appears to be the dominant limitation at low supply voltages). The typical extended swing of folded structures is not exploited in this circuit. The minimum $V_{DD}$ for the single-branch structure is $V_{DD\min} = V_{sat} + V_{GS1} + V_{GS3} + V_{swing} + V_{sat}$, and, for the folded structure, it is slightly lower; $V_{DD\min} = V_{sat} + V_{GS1} + V_{swing} + V_{sat}$. For a 0.18µm technology, assuming $V_{sat}$ = 250mV, $V_{GS1} = V_{GS3}$ = 450mV (to maximize $g_m$), and $V_{swing}$ = 400mV (the peak-to-peak single ended swing), the $V_{DD\min}$ for the folded case (1.35V) is only slightly lower than for the single-branch case ($V_{DD\min}$ = 1.8V) and does not justify doubling the power consumption in the folded structure (due to the doubling of the branches drawing current). Thus, the single-branch structure has lower power.

Finally, in addition to reducing power, the above cells feature these additional advantages:

• No parasitic poles are introduced, avoiding the power cost of pushing non-dominant singularities at high frequency.

• No common-mode feedback circuit is used (the output common-mode voltage is fixed to be $(V_{GS1} + V_{GS3})$ lower than the input common-mode voltage.

• Low output impedance (as a source follower the filter can drive a moderate resistive load or a switched-capacitor without substantially modifying the filter linearity and transfer function).

A 4th-order fully-differential low-pass filter for a WLAN receiver has been realized in a 0.18µm CMOS technology as a cascade of two single-branch cells and is shown in Fig. 19.5.2. The 1st cell is made up of PMOS transistors, while the 2nd one is made up of NMOS transistors. The use of cascading PMOS and NMOS structures compensates the input-to-output common-mode voltage difference, typical of a source-follower. All MOS devices have $L$ = 0.5µm to reduce problems caused by low output impedance. All capacitors are realized with digitally-controlled arrays. The filter transfer function pole is then programmable by ±40% with a 4b word; thereby compensating for variations in technology, temperature and parasitic capacitance. This means that, with tuning, the bias current ($I_o$) remains constant, fixing the $V_{ov}$ and, as a consequence, the loop gain and the linear range. Fig. 19.5.3 shows the nominal transfer function, which exhibits a 10MHz cut-off frequency. While the gain of the 1st cell (PMOS-based) is close to one, the gain of the 2nd cell (NMOS-based) is effected by the bulk transconductance (no double well was available in the process, disabling the cancellation of the NMOS bulk transconductance). This effect is well modeled and can also be reduced with a bulk connection of the NMOS devices.

Figure 19.5.4 shows the in-band IM3 for two 200mV$_{pp}$ tones at 3MHz and 4MHz at the output nodes. This corresponds to an in-band IIP3 of 17.5dBm as shown in Fig. 19.5.5. The 1dB compression point is 5dBm (i.e., 1.15V$_{pp_diff}$ from a 1.8V supply). In Fig. 19.5.6 the linearity has been evaluated in term of HD3, plotted as a function of the input amplitude at 3MHz. The HD3 is -40dB for a 600mV$_{pp_diff}$ input signal. The input-referred noise spectral density is about 7.5nV/√Hz (and 24µV$_{rms}$ as integrated input noise, giving a 79dB DR for -40dB HD3), thanks to the use of large values for $C_1$ and $C_2$; 85.3pF and 25.5pF for the 1st cell, and 71.4pF and 50.1pF for the 2nd cell, respectively. Using these capacitor values reduces the effect of parasitic capacitances. In addition, despite these large capacitors, the complete 4th-order filter only consumes 4.1mW (2.28mA@1.8V). For comparison, an active-$G_m$-*RC* [2] and a multipath active-*RC* cell with the same performance have been designed. The active-$G_m$-*RC* filter requires 45mA, while the multipath active-*RC* filter needs a much larger current. A micrograph of the fabricated circuit is shown in Fig. 19.5.7. The circuit uses 0.52mm$^2$ for two filters (I&Q topology), or 0.26mm$^2$ for each filter, whose largest part (>90%) is occupied by the capacitors.

*References:*

[1]I. Bouras, et al., "A Digitally Calibrated 5.15 - 5.825GHz Transceiver for 802.11a Wireless LANs in 0.18µm CMOS," *ISSCC Dig. Tech. Papers*, pp. 352-353, Feb., 2003.

[2] S. D'Amico, V. Giannini, A. Baschirotto, "A 1.2V-21dBm OIP3 4th-Order Active-gm-RC Reconfigurable (UMTS/WLAN) Filter with On-Chip Tuning Designed with an Automatic Tool," *Proc. European Solid-State Circuits Conf.*, pp 315-318, 2005.

[3] A. Baschirotto, U. Baschirotto and R. Castello, "High-Frequency CMOS Low-Power Single Branch Continuous-Time Filters," *Proc. IEEE Int. Symp. Circ. Syst.*, pp. II-557, II-580, 2000.

 

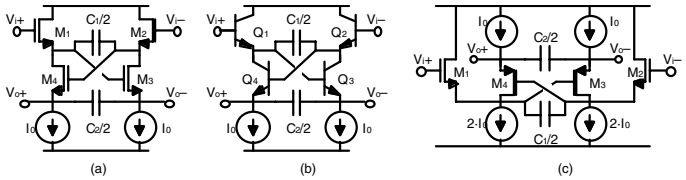


Figure 19.5.1: Basic 2nd-order continuous-time filter cells.

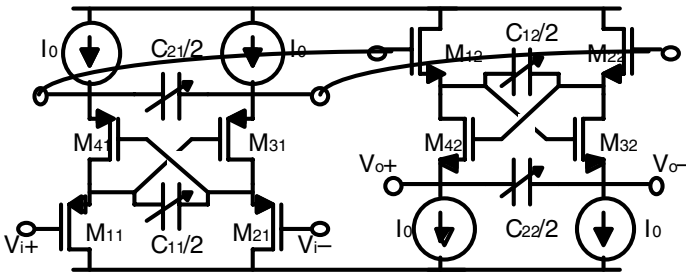

Figure 19.5.2: The 4th–order filter structure.

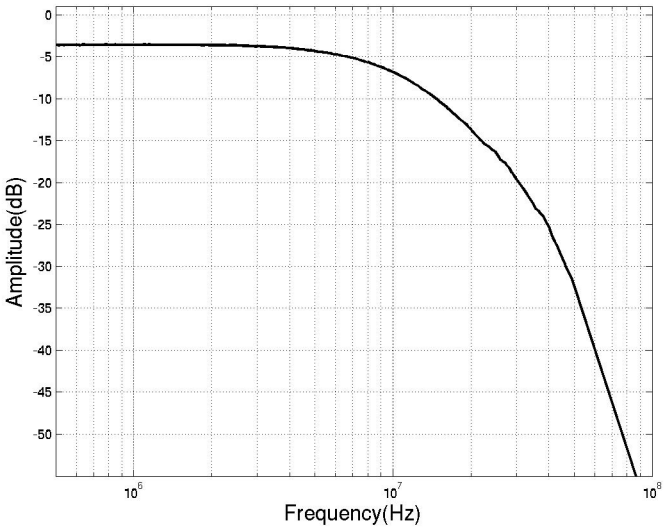


Figure 19.5.3: The filter transfer function.

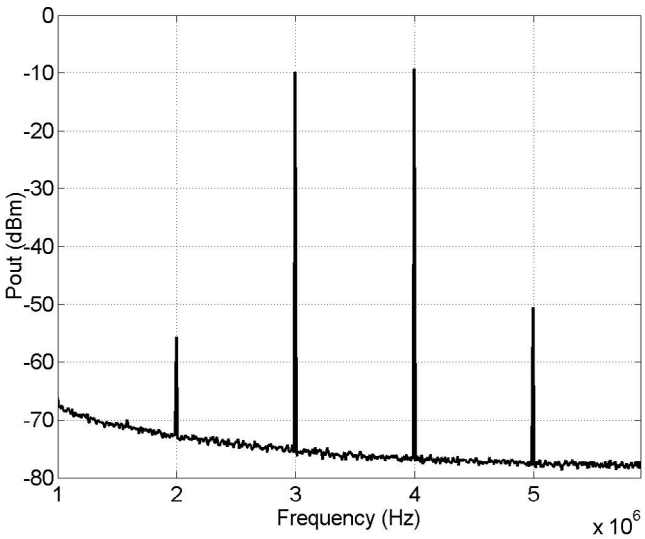


Figure 19.5.4: The in-band IM3.

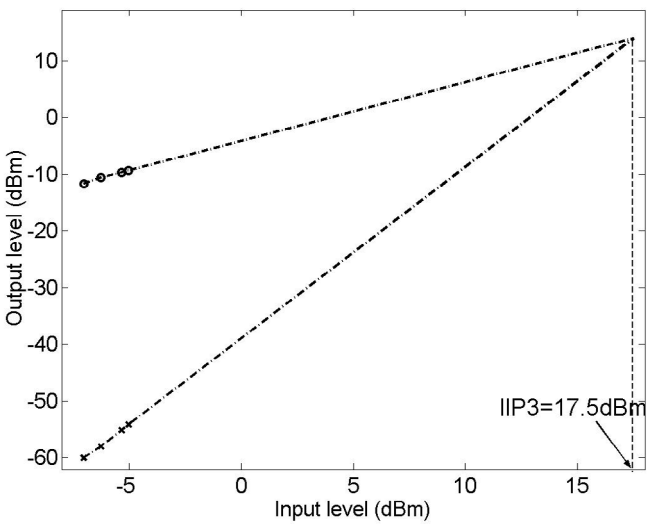


Figure 19.5.5: The filter IIP3.

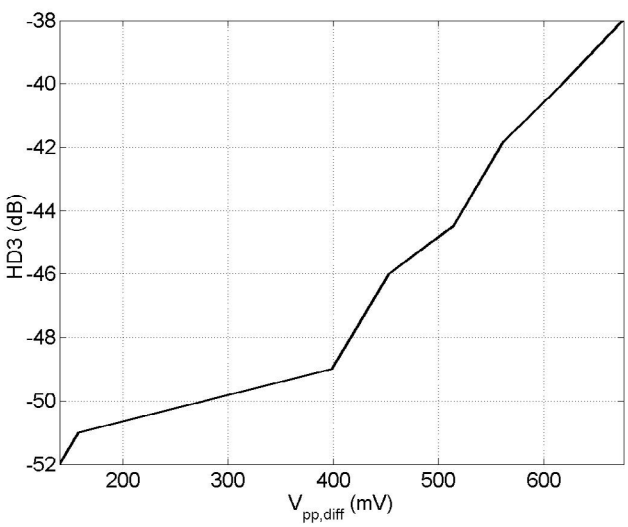


Figure 19.5.6: The filter HD3 versus input sine amplitude at 3MHz.

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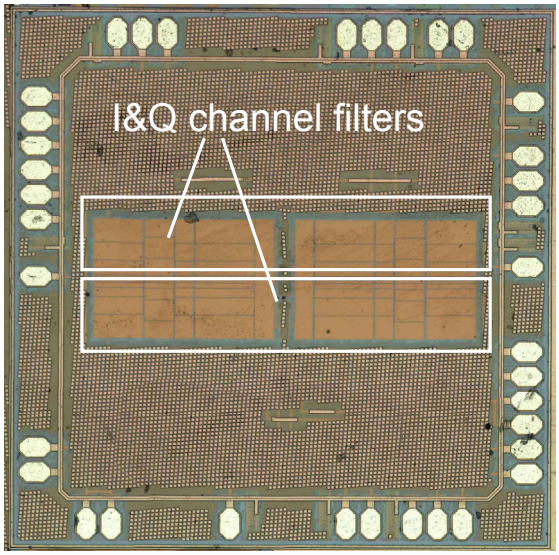


Figure 19.5.7: Chip micrograph.

 